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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,240	10/21/2003	Jung-Jin Kim	9903-073	6924

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EXAMINER	
TRAN, MAI HUONG C	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/691,240	KIM ET AL.	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *8-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 13-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/21/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

Application's election without traverse of Group I (Claims 1-7 and 13-22) drawn to a semiconductor device is acknowledged for prosecution in the subject application. Accordingly, claims 5-12 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Applicants have the right to file a divisional application covering the subject matter of the non-elected claims.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4 and 13-22 are rejected under 35 U. S. C. § 102 (e) as being anticipated by US Patent Application Publication No. 2003/0168725 to Warner et al.

Regarding to claim 1, Warner discloses a ball grid array package stack comprising a lower package 200 comprising a first circuit substrate 210 comprising a first substrate portion, a second substrate portion, and a third substrate portion (fig. 4); a first integrated circuit chip 201 attached on and electrically connected to a top surface 211 of the first substrate portion, a first molding resin 226 covering the top surface 211 of the first substrate portion and the first integrated circuit chip 201; the second substrate portion (fig. 4) being folded so that the third substrate portion (fig. 4) is positioned on the upper surface of the molding resin 226, and a larger number of subassemblies including folded substrates, packaged microelectronic elements may be included. The stack may be comprised of subassemblies that are identical with each other (page 5, [0060], and fig. 4) such as an upper ball grid array package comprising a second circuit substrate; a second integrated circuit chip attached on and electrically connected to a top surface of the second circuit substrate, interconnection terminals formed on a bottom surface of the second circuit substrate, and a ball grid array connecting the interconnection terminals to the third substrate portion of the first circuit substrate.

Regarding to claim 2, Warner discloses the ball grid array package stack comprising external connection terminals 259 formed on a bottom surface of the first substrate portion, the external connection terminals being distributed over the

bottom surface of the first substrate portion of the first circuit substrate 210 (page 4, [0054], and fig. 4).

Regarding to claim 3, Warner discloses the ball grid array package stack wherein the external connection terminals are solder balls (page 5, [0059], and fig. 4).

Regarding to claim 4, Warner discloses the ball grid array package stack wherein the lower package further includes metal wires 208 for electrically connecting the first chip 201 and the first circuit substrate 210 (page 5, [0056]), and a larger number of subassemblies including folded substrates, packaged microelectronic elements may be included. The stack may be comprised of subassemblies that are identical with each other (page 5, [0060]) such as the upper package further includes metal wires for electrically connecting the second chip and the second circuit substrate.

Regarding to claim 13, Warner discloses a stacked ball grid array package comprising a first integrated circuit 201 mounted on a first portion of a folded circuit substrate 210, the first integrated circuit being connected to a first array of connection balls 259, some of which are located under the first integrated circuit,

and a larger number of subassemblies including folded substrates, packaged microelectronic elements may be included. The stack may be comprised of subassemblies that are identical with each other (page 5, [0060], and fig. 4) such as a second integrated circuit positioned above a second circuit substrate, the second integrated circuit connected to a second array of connection balls located under the second circuit substrate, some of the second array of connection balls being located under the second integrated circuit, the second integrated circuit being positioned above the first integrated circuit, and a second portion of the folded circuit substrate that extends under, and is connected to, the second array of connection balls.

Regarding to claim 14, Warner discloses an integrated circuit package comprising a circuit substrate 210 comprising a first substrate portion, a second substrate portion, and a third substrate portion, the second substrate portion being folded approximately 180 degrees (fig. 4) so that the third substrate portion is positioned above the first substrate portion; a bottom ball grid package comprising a first integrated circuit 201 positioned on top of and connected to the first substrate portion, and first connection balls 259 positioned on the bottom of the first substrate portion; and a larger number of subassemblies including folded substrates, packaged microelectronic elements may be included. The stack may be

comprised of subassemblies that are identical with each other (page 5, [0060], and fig. 4) such as a top ball grid package comprising a second integrated circuit, a top substrate, and second connection balls, the integrated circuit being positioned on top of and connected to the top substrate and the second connection balls being positioned on the bottom of the top substrate, the top ball grid package being position above the bottom ball grid package so that the second connection balls are positioned on the top of and connected to the third substrate portion whereby both of the integrated circuits are connected to the circuit substrate.

Regarding to claim 15, Warner discloses the integrated circuit package wherein the connection balls are solder balls (page 5, [0059], and fig. 4).

Regarding to claim 16, Warner discloses the integrated circuit package wherein the first substrate portion comprises electrical connections 208 and the first connection balls 259 are connected to the electrical connections (page 5, [0056], and fig. 4).

Regarding to claim 17, Warner discloses the integrated circuit package and a larger number of subassemblies including folded substrates, packaged microelectronic elements may be included. The stack may be comprised of subassemblies that are

identical with each other (page 5, [0060], and fig. 4) such as the third substrate portion includes electrical connections and the second connection balls are connected to the electrical connections.

Regarding to claim 18, Warner discloses the integrated circuit package wherein the first substrate portion comprises electrical connections 208 and the first integrated circuit 23 is connected to the electrical connections (page 5, [0060], and fig. 4).

Regarding to claim 19, Warner discloses the integrated circuit package wherein the third substrate portion includes electrical connections and the second integrated circuit is connected to the electrical connections (page 5, [0056], [0060], and fig. 4).

Regarding to claim 20, Warner discloses the integrated circuit package wherein the first integrated circuit and the first substrate portion are covered with a molding resin 226 and the bottom of the third substrate portion is positioned on top of the molding resin (page 5, [0055], and fig. 4).

Regarding to claim 21, Warner discloses the integrated circuit package further comprising metal wires connecting the first integrated circuit to the first

substrate portion and metal wires connection the second integrated circuit to the top substrate (page 5, [0056], [0060] and fig. 4).

Regarding to claim 22, Warner discloses a large number of subassemblies including folded substrates, packaged microelectronic elements may be included. The stack may be comprised of subassemblies that are identical with each other (page 5, [0060], and fig. 4) such as an integrated circuit package comprising a plurality of integrated circuits each integrated circuit being connected to an associated array of connection balls, some of which are located under the associated integrated circuit, the integrated circuits being positioned in a vertical stack, a plurality of folded circuit substrates, each folded substrate being folded so that there is a second substrate portion on top of a first substrate portion,
each of the folded substrates comprising one of the integrated circuits position on top of and connected to its first portion and the connection balls that are associated with a different integrated circuit positioned on top of and connected to the top of its second portion, whereby multiple integrated circuits can be stacked and connected with some of the connection balls associated with each particular integrated circuit being located directly underneath the particular integrated circuit.

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 5 is rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent Application Publication No. 2003/0168725 to Warner et al. (hereinafter Warner) in view of US Publication No. 2002/0044423 to Primavera et al. (hereinafter Primavera).

Regarding to this claim, Warner discloses the ball grid array package stack, wherein the first circuit substrate 210 has first ball pads 216 formed in the first portion to receive the external connection terminals (page 5, [0056], and fig. 4). Warner does not disclose the second ball pads formed in the third portion to receive the interconnection terminals, and connection lines connecting the first and the second ball pads.

However, Primavera discloses the second ball pads 24 formed in the third portion to receive the interconnection terminals, and connection lines 44 connecting the first 24 and the second ball pads 34 (page 3, [0046], figs. 3 and 6B).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the second ball pads formed in the third portion to receive the interconnection terminals, and connection lines connecting the first and the second ball pads, as taught by Primavera in order to provide an inexpensive and reliable package for an IC chip or other component which requires minimal mounting real estate (page 1, [0009], [0010]).

Claims 6 and 7 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent Application Publication No. 2003/0168725 to Warner et al. (hereinafter Warner) in view of US Publication No. 2002/0044423 to Primavera et al. (hereinafter Primavera) and further in view of U.S Patent No. 6,576,493 to Lin et al. (hereinafter Liu).

Regarding to claim 6, Warner in view of Primavera discloses the claimed invention except for the ball grid array package stack wherein the first circuit substrate further has a base layer on which the first and the second ball pads and the connection lines are formed, and a coating layer covering the base layer and the connection lines and having pad openings through which the first and the second ball pads are exposed. However, Lin discloses the substrate has a base layer 122 on which the ball pads 146 and the connection lines 170 are formed, and a coating layer 124 covering the base layer 122 and the connection

lines 170 and having pad openings 154 through which the ball pads 146 are exposed (col. 10, lines 28-49, and figs. 1K, 3K).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the substrate that has a base layer on which the ball pads and the connection lines are formed, and a coating layer covering the base layer and the connection lines and having pad openings through which the ball pads are exposed, as taught by Lin in order to provide a low cost, high performance, high reliability package (col. 4, lines 20-21).

Regarding to claim 7, Primavera discloses the ball grid array package stack wherein the external connection terminals 36 are formed on the first ball pads 34 through the pad openings, and the interconnection terminals 26 are joined to the second ball pads 24 through the pad openings (page 3, [0048], and fig. 6B).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mai-Huong Tran whose telephone number is (571)272-1796. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mai-Huong Tran
Examiner
Art Unit 2818